Temperature and Power Predictions for Flight-testing the Free Molecule Micro-Resistojet*†

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IEPC-01-232

The Free Molecule Micro-Resistojet (FMMR) will be flight-tested on the Three Corner Sat (3CS) constellation in 2003. The FMMR is a MEMS fabricated resistojet. The goal of this flight test is to collect power characteristic of two types of FMMR heater chip operating in the LEO environment. The first heater chip has a silicon nitride coating on the backside, and the second type has a gold coating on top of the silicon nitride layer. A series of experiments has been carried out in laboratory to predict the chip performance in space. Testing at high vacuum has shown that the maximum chip temperature of the nitride chip is 521K at 1.950W, and that of the gold chip is 540K at 1.987W when operated at 12 VDC, nominal bus voltage on the 3CS spacecraft.

Acronyms

3CS	Three Corner Satellite
AFRL	Air Force Research Laboratory
ASU	Arizona State University
DSMC	Direct Simulation Monte Carlo
EU	Engineering Unit
FMMR	Free Molecule Micro-Resistojet
JPL	Jet Propulsion Laboratory
LEO	Low Earth Orbit
LN2	Liquid nitrogen
LSN	Low Stress Nitride
MEMS	Micro-Electro-Mechanical Systems

Introduction

FMMR Background

The FMMR is a MEMS fabricated resistojet. For a typical LEO microsatellite, FMMR proposes to use ice as propellant and utilizes the vapor pressure of ice to create a free molecular flow environment inside the device. Numerical simulations using the Direct Simulation Monte Carlo (DSMC) have shown that for a water propellant with a stagnation pressure of about 195Pa, the optimal wall temperature of the nozzle is 600K [1]. This operating pressure can produce a thrust per unit slot length of approximately 10mN/m [2], [3]. Different thrust levels can be achieved by adjusting the stagnation pressure or by changing the propellant tank temperature. To meet the requirement of small impulse-bit for fine attitude control, FMMR can

* Presented as Paper IEPC-01-000 at the 27th International Electric Propulsion Conference, Pasadena, CA, 15-19 October, 2001.

produce very low (μN-level) thrusts. Thus, it alleviates the imminent need for fast-actuating valve.

In the course of the development of the FMMR, four versions of the first generation heater chip have been manufactured, tested and characterized to various degrees in the laboratory. These chips have demonstrated the feasibility of the idea made possible by current MEMS technology. In addition, these prototypes have provided valuable data for designing the flight FMMR based on terrestrial testing [2]. Currently, a numerical model of the FMMR heater chip is being developed using a commercial heat transfer code[‡], ABAQUS, coupled with DSMC. It is hoped that a reliable numerical model will greatly reduce the cost and time required to design any future FMMR heater chips.

The objectives of this paper are to describe and summarize the ground-based testing of the current FMMR heater chip that will be flight-tested on a LEO microsatellite constellation.

Flight-test Background

The FMMR first flight-test is a joint project among the Air Force Research Laboratory (AFRL), the Jet Propulsion Laboratory (JPL) and the Arizona State University (ASU). AFRL was responsible for providing the hardware and testing facility for FMMR. The Microdevices Laboratory at JPL provided for the fabrication of the FMMR heater chips. ASU is responsible for characterizing, testing and designing the first FMMR flight experiment and to provide the spacecraft bus for the flight-test.

The 3CS constellation is a three-satellite constellation built by ASU, University of Colorado (Boulder) and the New Mexico State University. It is part of the University Nanosatellite Program managed by the AFRL. The delivery date of the 3CS stack to the AFRL is December 1, 2001, and the constellation will be launched by the Space Shuttle in 2003. The primary mission objectives are to perform stereoscopic imaging, virtual formation flying and distributed and automated operations [4], [5], [6]. In addition, two of the three 3CS spacecrafts will carry one FMMR experiment unit each. Due to the tight project schedule and the time required for the feed system development, only the FMMR heater chip will be flown on the 3CS constellation. Since neither the feed system nor the propellant are intended to be tested on this first flight, no thrust will be produced on-board the spacecrafts. The originally planned 3CS FMMR mission is documented in other sources [7], [8].

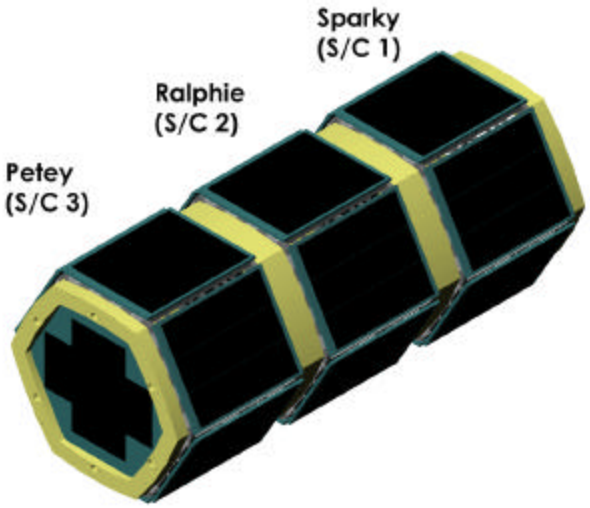

Figure 1 – 3CS spacecrafts in stack configuration.

All three 3CS spacecrafts are identical except that the bottom satellite (in the deployment stack configuration) does not carry a FMMR experiment unit and has a different deployment ring than the other two. The external hexagonal envelope of the spacecraft measures 46cm point-to-point and 27cm high. Each spacecraft weighs approximately 17kg. Figure 1 is a depiction of the 3CS stack, and Figure 2 is a depiction of an individual satellite. The stack will be ejected from the Shuttle at a minimum altitude of 350km. The constellation is expected to have a nominal on-orbit life of two months.

[‡] ABAQUS has many other analytical capabilities. We are, however, only interested in using the heat transfer part of the code.

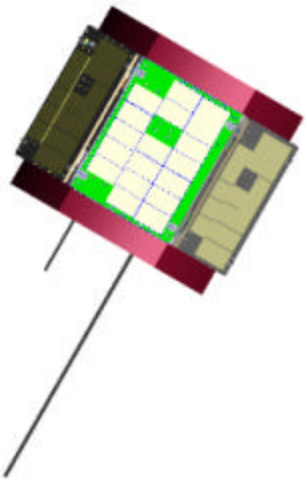

Figure 2 – 3CS spacecraft.

3CS FMMR Experiment

The objectives of the 3CS FMMR experiment are to test the chips survivability through launch and to collect power consumption data of the chips when operating in the LEO environment. Each FMMR experiment unit consists of two different FMMR heater chips. They are physically identical except that one of them has an extra layer of gold evaporated on the backside. The difference in emissivity will cause different radiation heat loss for the chips; hence, they will have different power consumption and surface temperature.

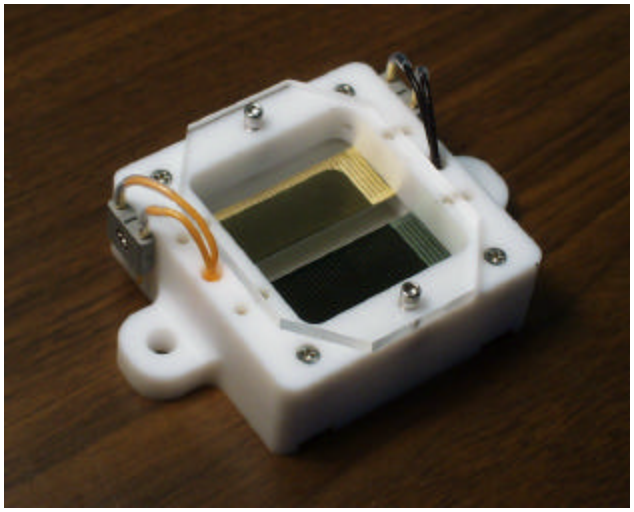

Figure 3 – 3CS FMMR experiment unit. The acrylic protective cover will be removed before flight.

Figure 3 is a picture of the FMMR experiment unit. Figure 4 is a depiction of the FMMR experiment unit mounted on the spacecraft structure.

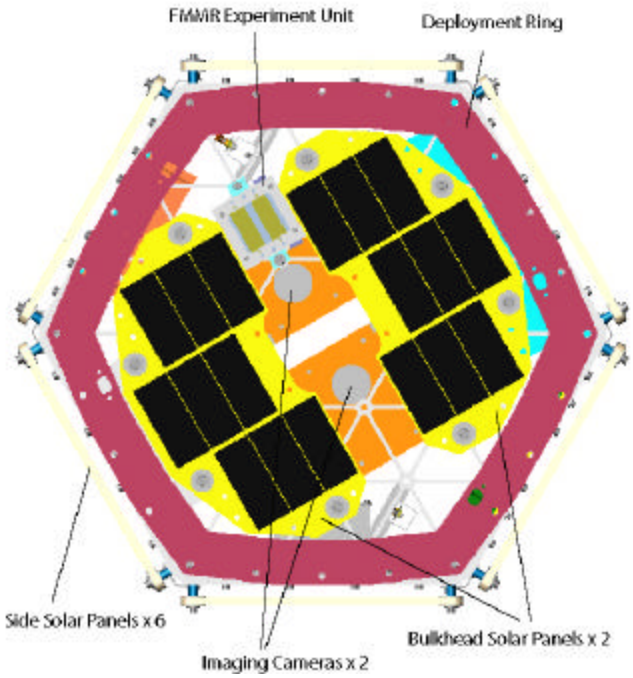

Figure 4 – Components placement on the 3CS spacecraft bottom bulkhead. The FMMR experiment unit is placed between the two solar panels in the top left vertex. The outer rim is part of the intersatellite deployment system, the LightBand.

The housing for the chips is machined from virgin Teflon because of its low thermal conductivity. The outside dimension measures 5 x 7 x 2cm, and each unit has total mass of 80g. The chips will be operated at the satellite bus voltage of 12VDC nominal and 15VDC maximum. The duty cycle of each chip is at a minimum of 10-minutes per orbit. Voltage and current data will be collected at a minimum frequency of 1Hz for the duration of the experiment operation. Experimental data will be downloaded from the satellite to the various ground stations established at the three universities.

FMMR Heater Chip Characterization

Theory

The FMMR produces thrust through the transfer of energy from the heated slot walls at T_w to propellant

gas molecules at T_i. Assuming free molecular flow and full accommodation of the propellant molecules on the heated walls, the thrust generated is

$$Thrust = \frac{n_p k}{2}\sqrt{T_w T_i}\, A_s \qquad (1)$$

where n_p is the propellant number density inside the microthruster, k is the Boltzmann's constant, and A_s is the slot area [9]. As suggested by the equation, accurate knowledge of the wall temperature is vital in calculating the thrust generated.

To estimate and understand the temperature distribution on the FMMR heater chip, one can begin by carrying out an energy balance analysis on the FMMR heater chip.

$$\dot{E}_{in} + \dot{E}_{generated} = \dot{E}_{out} + \dot{E}_{stored} \qquad (2)$$

Since there is no thermal or mechanical energy entering the unit, $\dot{E}_{in}$ is zero. The rate of change of energy generated inside the unit is due to the electric resistance heating (Joule heating) of the heating element on the chip. The rate of change of energy leaving the chip is comprised of the radiation heat loss and the conduction heat loss to the environment. The rest of the analysis would be easier to envision by transforming the energy balance equation into a differential equation involving temperature. The brief derivation in the following is taken out of references [10] and [11].

Consider a chip element of dimension Δx, Δy, and Δz (see Figure 5). The energy balance is written as

$$Q_x^k + Q_y^k + Q_z^k + Q^d = Q_{x+\Delta x}^k + Q_{y+\Delta y}^k + Q_{z+\Delta z}^k + Q^{st} \qquad (3)$$

where Q_x^k is the heat rate conducted at x across the y-z plane, and similarly for Q_y^k and Q_z^k. Likewise, the same applies for $Q_{x+\Delta x}^k$, $Q_{y+\Delta y}^k$ and $+Q_{z+\Delta z}^k$ at x+Δx, y+Δy and z+Δz.

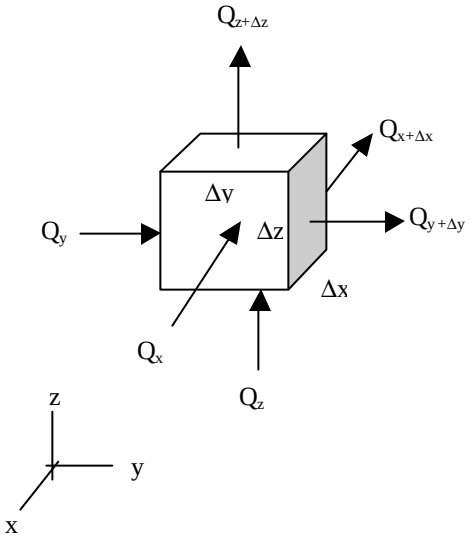

Figure 5 – Heat conduction in a volumetric element of the chip in Cartesian coordinates.

Fourier's law of conduction gives

$$Q_x^k = -k_x \frac{\partial T}{\partial x}(\Delta y \Delta z) \qquad (4a)$$

$$Q_y^k = -k_y \frac{\partial T}{\partial y}(\Delta x \Delta z) \qquad (4b)$$

$$Q_z^k = -k_z \frac{\partial T}{\partial z}(\Delta y \Delta x) \qquad (4c)$$

where κ is the thermal conductivity of the material dependence of direction.

Using the Taylor expansion for the heat conduction rate at ξ+Δξ,

$$Q_{x+\Delta x}^k = Q_x^k + \left.\frac{\partial Q_x^k}{\partial x}\right|_x \Delta x + HOT \qquad (5)$$

Discarding the higher order terms, the six heat conduction rate terms can be rewritten as

$$\left(\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right)\right)(\Delta x \Delta y \Delta z)$$

The rate of heat generation due to Joule heating on the element is

$$Q^{d}_{Joule} = (dV)_{element} I \qquad (6)$$

where dV is the voltage drop across the portion of heating element on the chip element. Since voltage equals current times resistance, and resistance is dependent on temperature, (6) becomes

$$Q^{d}_{Joule} = I^{2} R_{element} \qquad (7)$$

The rate of radiation heat loss at the element surface can be expressed as

$$Q_{rad} = e s (T^{4}_{element} - T^{4}_{env}) A_{element} \qquad (8)$$

where ε is the emissivity of the chip surface, σ is the Stephen-Boltzmann constant, $A_{element}$ is the area of the element radiating surface, $T_{element}$ is the surface temperature of the element, and T_{env} is the temperature of the environment to which the element radiates.

The rate of heat stored is

$$Q^{st} = \left(r c_p \frac{\partial T}{\partial t} \right) \Delta x \Delta y \Delta z \qquad (9)$$

where ρ is the material density of the element and c_p is the specific heat capacity at constant pressure.

Finally, assuming the thermal conductivity is constant, combining all the terms and dividing by the elemental volume, the governing equation describing the heat transfer of the chip element becomes

$$\left(I^{2} R_{element} - e s (T^{4}_{element} - T^{4}_{env}) A_{element} \right) \frac{1}{\Delta Vol} + k \nabla^{2} T_{element} = \left(r c_p \frac{\partial T}{\partial t} \right) \qquad (10)$$

This partial differential equation is second order in space and first order in time. It is nonlinear due to the radiation term. It is also coupled between the thermal and electrical system because of the temperature-dependent resistance of the heating element. This equation will be tackled in the numerical modeling of the FMMR heater chip. However, it is introduced in this paper to illustrate that behind the findings of the experiment is an intricate system of heat transfer "accounting."

Physical Properties

The FMMR heater chip (version Mark I.4) measures 13 x 42mm and 400μm thick. The mass of the chip is about 0.5g. It is micro-machined from Low Stress Nitride (LSN) silicon wafer. As the name suggests, this type of wafer has a 5000Å layer of silicon nitride (Si_3N_4), an electrical insulator, deposited on both sides. One side of the chip has an evaporated metal serpentine pattern, which forms the heating element of the chip. The heating element is made up of three layers of metal thin film. First, there is a 300Å layer of chromium that acts as a bonding layer. Second, there is a 600Å layer of platinum that acts as a diffusion barrier. Third, there is an 8000Å layer of gold which acts as the main current-carrying layer. The resistance of the heater is about 40Ω at room temperature.

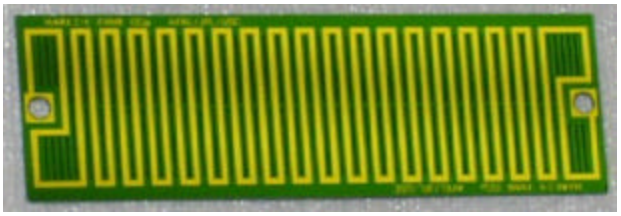

Figure 6 – Heating element on the FMMR heater chip.

A total of 50 slots are etched on the chip in between the heating element. These slots are essentially the expansion nozzles of the microthruster. Each slot is 100μm wide and the length varies between 3 to 5mm. The micro-machining and manufacturing of the heater chip is reported in references [1] and [12]. Figure 6 shows the heater side of the chip, and the backside of the nitride chip is shown in Figure 7.

For the gold FMMR heater chip, instead of exposing the silicon nitride on the backside, it is deposited with an 8000Å thick of gold by evaporation, which theoretically reduces the emissivity of the backside from 0.5 to 0.02.

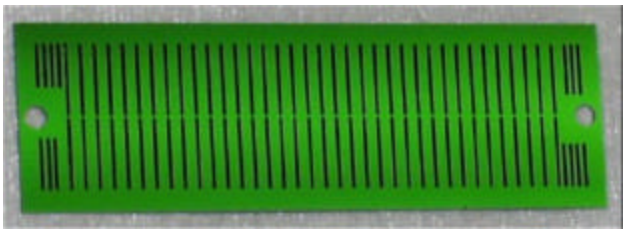

Figure 7 – Backside of the FMMR heater chip.

Experiment Objectives

The heater chip characteristics of interest are the surface temperature and the overall power consumption. Three major sets of experiment have been performed in order to characterize the above properties. The goal of the first set (Set1) of experiments was to determine the chip's heat transfer sensitivity to different high vacuum. The second set (Set2) collects temperature and power data of the chip at high vacuum pressure (~1e-6Torr), radiating to a room temperature thermal shroud at various DC voltages. The third set (Set3) is a replica of the second set, except that the chip was radiating to the thermal shroud whose surface temperature was held at or less than 100K. **Table 1** is a test matrix of the FMMR heater chip.

Table 1 Test Matrix to Characterize the FMMR Heater Chip

Chip	**Nitride**	**Gold**
Shroud Temperature		
Room	*Set1, Set2*	*Set2*
LN2	*Set3*	*Set3*
Pressure (Torr)		
1e-4	*Set1*	-
1e-5	*Set1*	-
1e-6	*Set1, Set2*	*Set2*
1e-7 or lower	*Set3*	*Set3*
Power Supply Voltage (V)		
5	*Set2, Set3*	*Set2, Set3*
7.5	*Set2, Set3*	*Set2, Set3*
8.5	*Set2, Set3*	*Set2, Set3*
10	*Set2, Set3*	*Set2, Set3*
12	*Set2, Set3*	*Set2, Set3*
13.5	*Set2, Set3*	*Set2, Set3*
15	*Set1, Set2*	*Set2*

Experiment Setup

The heater chip was first secured on a Teflon fixture with two #0-80 stainless steel nut and screw assemblies. They also served as the electrical contact between the chip and the power supply with the power wire sandwiched between the nut and the screw head. A small amount of AI Technology silver epoxy EG8050 was applied between the chip and the nut and about the #0-80 assembly to ensure good electrical contact.

Five J-type thermocouples were used to record the slot temperature at different locations on the chip. Because of physical symmetry of the heater chip, thermocouples were placed on only half of the chip. Thermocouple placements are illustrated in Figure 8 for the nitride chip and Figure 9 for the gold chip. The thermocouple tip is round and has diameter of 0.005 inch. They were flattened with a spot-welder and then inserted between the slots. Despite the snug fit of the thermocouple in the slot, a small amount of high-temperature epoxy was applied on the thermocouple and the chip to prevent any longitidinal movement in the slot and to improve contact. Figure 10 is a picture showing the nitride heater chip mounted on the top Teflon housing with several thermocouples inserted in the slots.

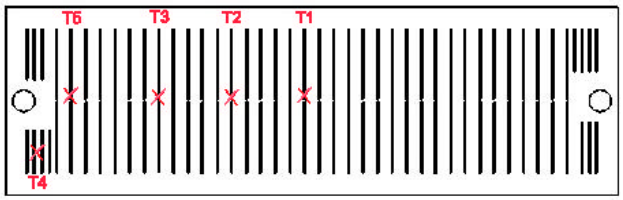

Figure 8 – Thermocouple location on the nitride FMMR heater chip.

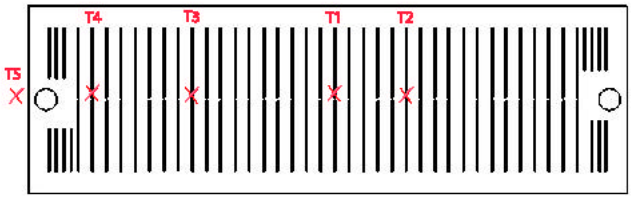

Figure 9 – Thermocouple location on the gold heater chip. Thermocouple T5 was mounted on the housing and measured the temperature of Teflon immediately next to the chip.

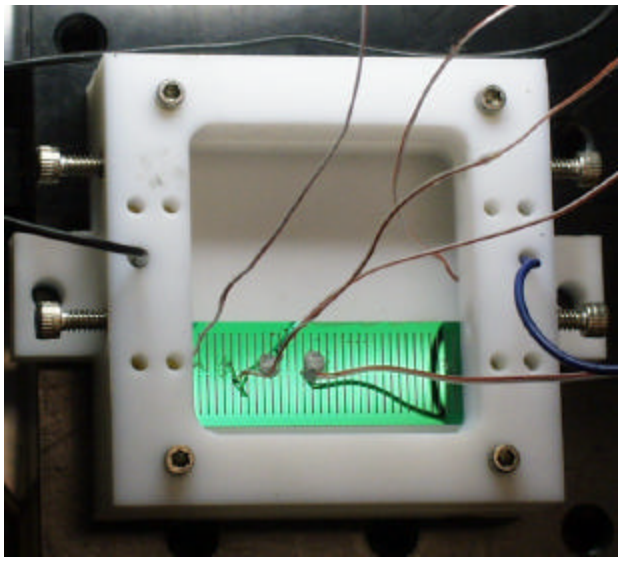

Figure 10 – Nitride heater chip laboratory test setup. The nitride chip was secured in the Teflon housing, and four thermocouples were inserted in the slots.

After securing the heater chip on the top housing, the top housing subassembly is attached to the bottom housing. The entire experiment unit is then placed inside a vacuum chamber (Figure 11) that is operated by a turbo-molecular pump and a mechanical pump. A toggle valve-needle valve system is used to bleed in air to control the pressures in the chamber for the Set1 experiments. A copper-aluminum thermal shroud with inner diameter of six inches is incorporated to the vacuum chamber for the Set2 and Set3 experiments. The shroud forms a closed loop system for circulating liquid nitrogen, or other fluid of choice, inside the chamber. This process enables the chip to radiate to an environment of reasonably uniform surface characteristics and temperature.

Data Acquisition

Figure 12 is a circuit diagram showing the FMMR experiment setup. Data collected include the thermocouple readings, voltage across the heater chip, and voltage across the shunt resistor. The shunt resistor was used to measure the current in the circuit whereby the power consumption of the chip could be calculated by

$$P = VI = I^2 R \qquad (11)$$

Figure 11 – Vacuum chamber setup.

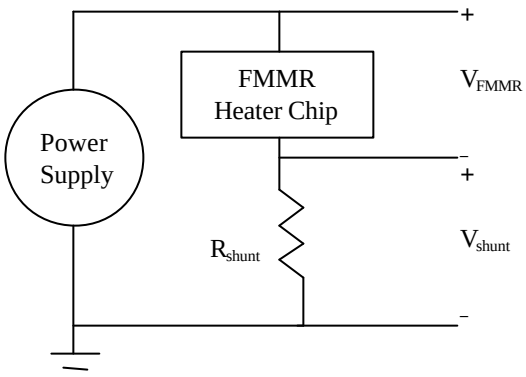

Figure 12 – Circuit diagram for the laboratory testing of the FMMR heater chip.

Instrument Calibration & Accuracy

The data acquisition system is a 24-bit system. The input voltage range is 0 to 15V. The accuracy is up to 5 decimal places. Thermocouples with the data acquisition system were calibrated in an oil bath from 273 to 500K using a high temperature thermometer.

The accuracy of the thermocouple measurement is ±0.5K. The consistency of the power supply had also been checked. In a voltage-limited setting, the voltage drop over a 60-minute period is less than 1%.

Test duration was set to be 60 minutes during which the power supply voltage was held constant and current unlimited. The state variables of interest were the five thermocouple measurements, voltage drop across the heater chip and voltage drop across the shunt resistor. The shroud temperature was also monitored with a K-type thermocouple. Due to the limitation of the noise reduction component in the data acquisition system, the acquisition frequency was limited to about 0.3Hz (about one sample of all the channels every 3 seconds).

Data Reduction

Each experiment was repeated 3 to 4 times to form an ensemble. The ensemble average was used in the general result and discussion of the characteristics of the chip. The error in the result is estimated using the following method

$$Error = \pm\sqrt{s^{2} + (DAQaccuracy)^{2}} \qquad (12)$$

where σ is the standard deviation of the ensemble [13].

Results & Discussion

General Characteristics

Figure 13 is a typical temperature and power plot of the heater chip with respect to time. The last 10-minute of data was averaged and used to describe the steady state characteristics of the chip.

The temperature of the chip changes rapidly in the first minute after powering. The time constant (60% of steady state value) is about 45 seconds. The temperature is within 5% of the steady state value in about 5 minutes. This behavior is independent of the voltage supplied and is very consistent.

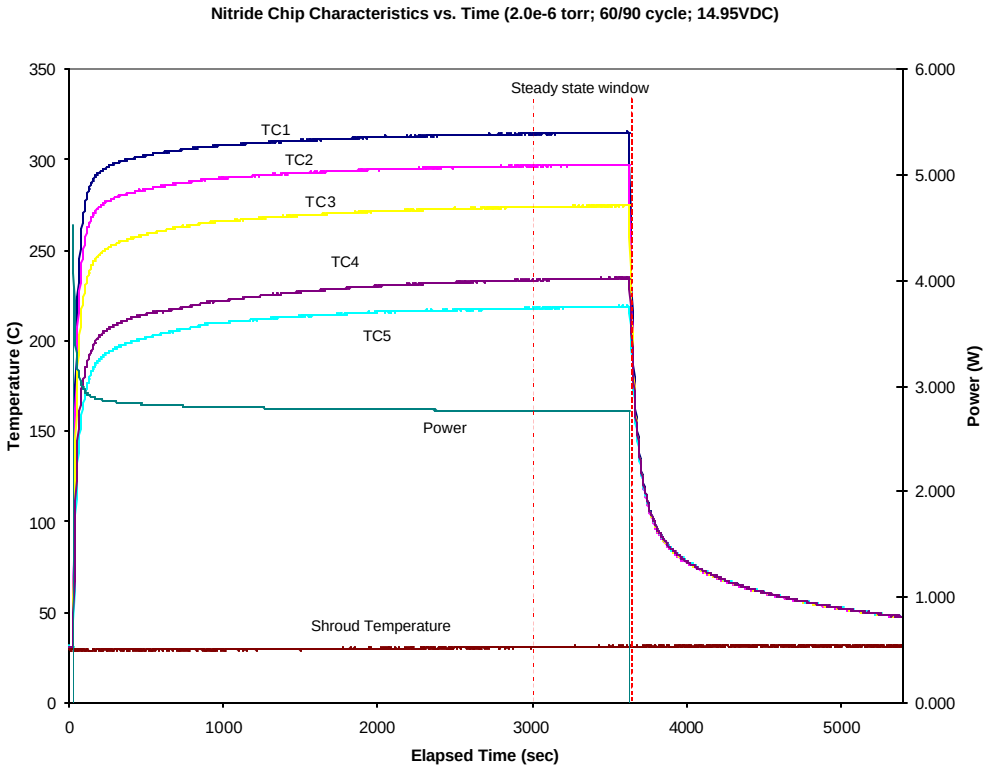

Figure 13 – Typical temperature and power characteristics of the nitride heater chip.

Set1: High Pressure Sensitivity

The nitride heater chip has shown no sensitivity to pressure variations in the high vacuum regime (from 1e-6Torr to 1e-4Torr) when operate at 15VDC. Figure 14 is a plot summarizing the result of the Set1 experiments. The average maximum temperature is 580K. The error in the data is ±1K.

The ambient and medium vacuum results illustrate the significant role of convection heat loss to the environment. Comparing the high vacuum case and the ambient case, about 50% of the input power is lost to the environment due to convection.

To eliminate the effects of convective heat transfer, it is best to maintain a vacuum at or lower than 1e-5Torr. Although at this pressure the gas molecules number density is still in general three to four orders of magnitude higher than in LEO, the effects of heat conduction by gas molecules is apparently insignificant.

One surprising but important discovery is the temperature gradient across the long side of the heater chip. At 15VDC, there could be as much as 80K difference between the center of the chip and part of the chip that is in contact with the Teflon housing. This could be a heat transfer characteristic of the chip due to the distribution of the heating element. On the other hand, the gradient could be driven by the conduction heat loss to the Teflon, although it has a very low thermal conductivity (about 0.25W/m-K) and the area in contact appears to be small. Besides performing additional experiments to investigate the cause, this observation would be better understood through numerical modeling of the problem, particularly by applying the appropriate boundary conditions and through parametric studies. The characteristics of the temperature gradient are important because they identify better assumptions than uniform surface temperature when carrying DSMC mass flow and thrust calculations.

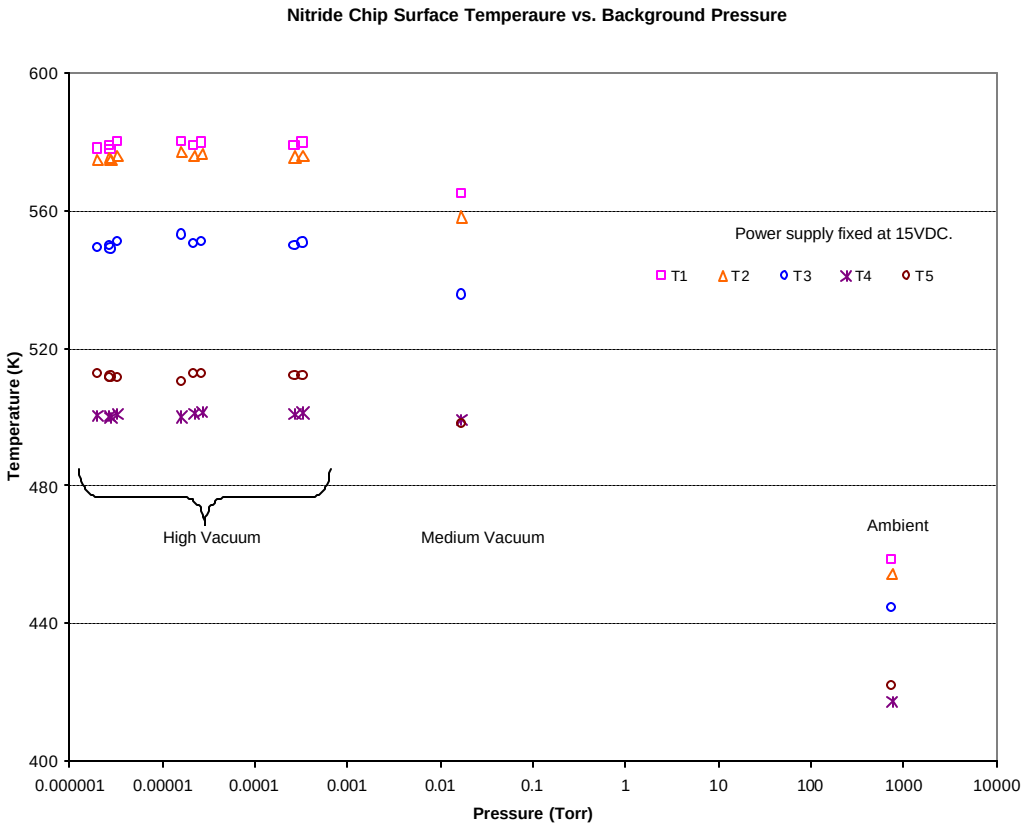

Figure 14 – Nitride chip surface temperature as a function of background pressure.

Set2: Room Temperature, High Vacuum Power Variation

The result of the nitride chip operating at various voltages in high vacuum (1e-6Torr < background pressure < 5e-6Torr) inside the thermal shroud at room temperature is summarized in Figure 15. The result of the gold chip is displayed in Figure 16.

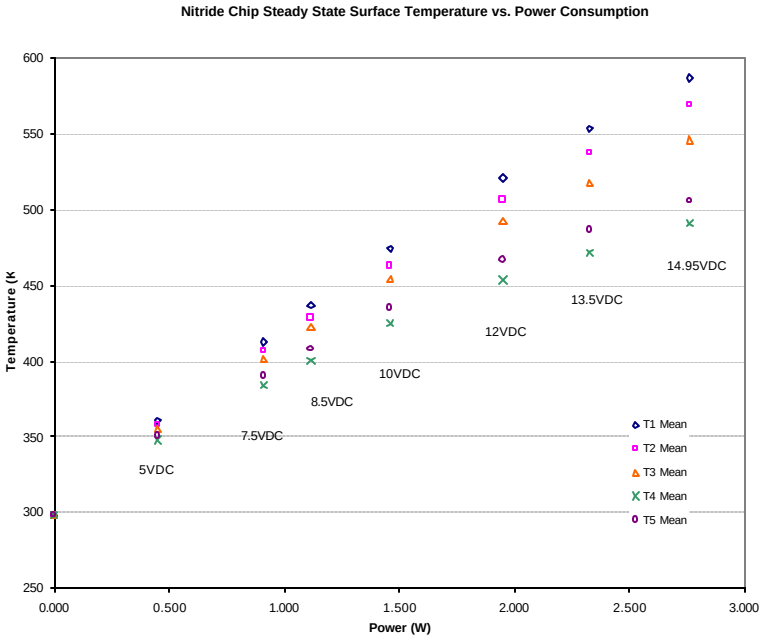

Figure 15 – Nitride chip surface temperature as a function of input power at high vacuum with the shroud temperature held at room temperature.

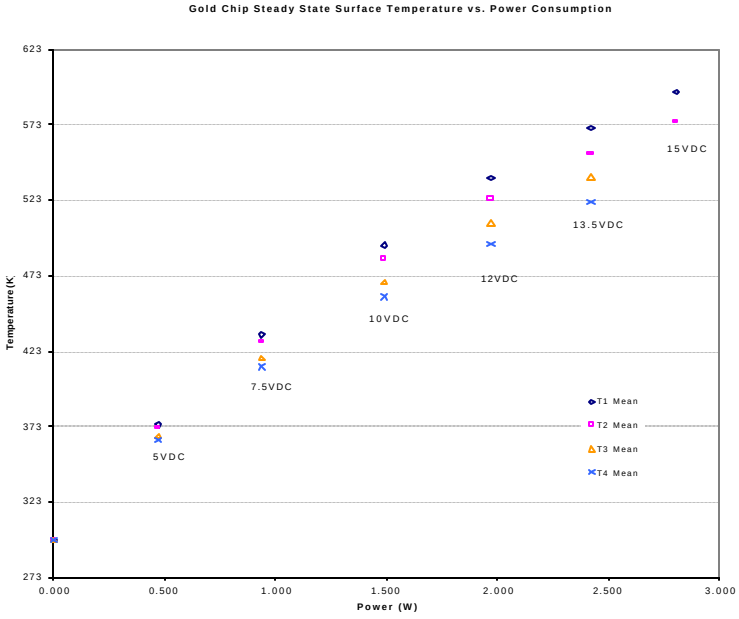

Figure 16 – Gold heater chip surface temperature as a function of input power at high vacuum with the shroud temperature held at room temperature.

The chip surface temperature varies with input power nonlinearly, and the relationship can be approximated with a second order polynomial, $y = a_2x^2 + a_1x + a_o$. Figure 17 shows the chip center temperature as a function of input power for the gold and the nitride chip. The error in temperature and power are also displayed on the plot. Temperatures at other location of the chip follow the same qualitative behavior, though they are not displayed individually in this paper. The polynomial coefficients, the correlation coefficient and the temperature error in the data are listed in **Table 2** and **Table 3** for the nitride and the gold chip respectively.

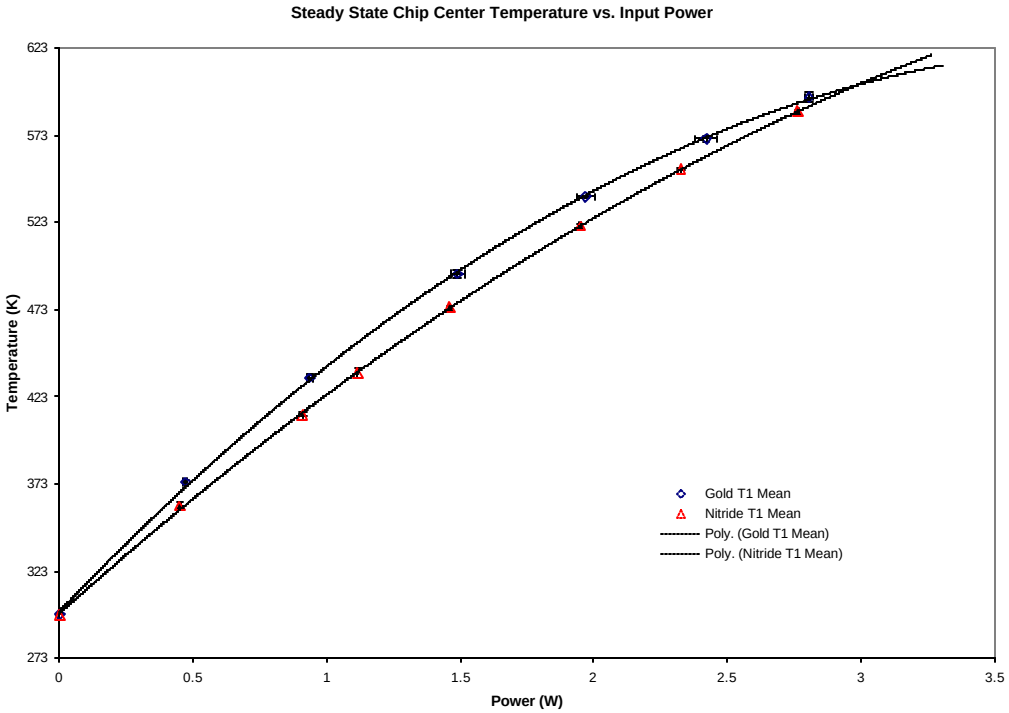

Figure 17 – Variation of chip center temperature as a function of input power at steady state.

Table 2 – Second Order polynomial coefficients for fitting the nitride chip surface temperature as a function of input power.

TC	a_2 (K/W^2)	a_1 (K/W)	a_o (K)	R^2
1	-12.069	137.42	299	.9999
2	-11.222	128.33	299	.9998
3	-12.855	124.32	299	.9997
4	-13.975	113.32	299	.9997
5	-12.941	104.32	300	.9997

Table 3 – Second Order polynomial coefficients for fitting the gold chip surface temperature as a function of input power. TC5 (thermocouple number 5) is excluded in the table because it was used to record the temperature of the Teflon.
*Thermocouple 3 and 4 were not available for the 15VDC ensemble set.

TC	a_2 (K/W^2)	a_1 (K/W)	a_o (K)	R^2
1	-19.785	160.05	300	.9997
2	-20.463	154.54	300	.9996
3*	-18.382	142.21	300	.9993
4*	-18.812	136.15	301	.9990

Although a second order polynomial was used to approximate the chip surface temperature as a function of input power, the mathematical correlation may not convey the most accurate physical relationship. The chip surface temperature should

increase monotonically with increasing input power and should not decrease with increasing power because of conservation of energy. The value of establishing some sort of mathematical relationship between the two variables is to enable slight extrapolation of the data into regime where no test result is available. For instance, it is possible to predict the amount of power required to heat the chip up to 600K using the mathematical correlation. The fit of the data indicates that in order for the center of the chip to reach 600K, it would require 2.935W for the gold chip, and 2.961W for the nitride chip.

The gold chip is more power efficient than the nitride chip for most of the temperature range in the experiment. However, its performance appears to decline at high temperatures. This could be caused by the temperature-dependency of the thin film material thermal properties, in particular, emissivity and conductivity [14], [15]. Due to the highly coupled heat transfer modes, it is very difficult to identify the dominant factor from this set of experimental data. Again, this would be another problem that the numerical model might provide an explanation through parametric study. Nevertheless, one can still estimate the power savings based on the average temperature on the chips from the experimental data. The average temperature per slot (excluding those in contact with Teflon) is calculated from

$$Tavg = \frac{1}{\frac{1}{2}L} \int_0^{\frac{1}{2}L} T(x)dx \qquad (13)$$

where T(x) is a second order polynomial fit of the temperature distribution based on the slot location with Figure 18 showing the nitride chip surface temperature distribution and Figure 19 for the gold chip. Figure 20 is the average chip surface temperature as a function of input power at steady state. The gold chip obviously is more power efficient from the average temperature perspective.

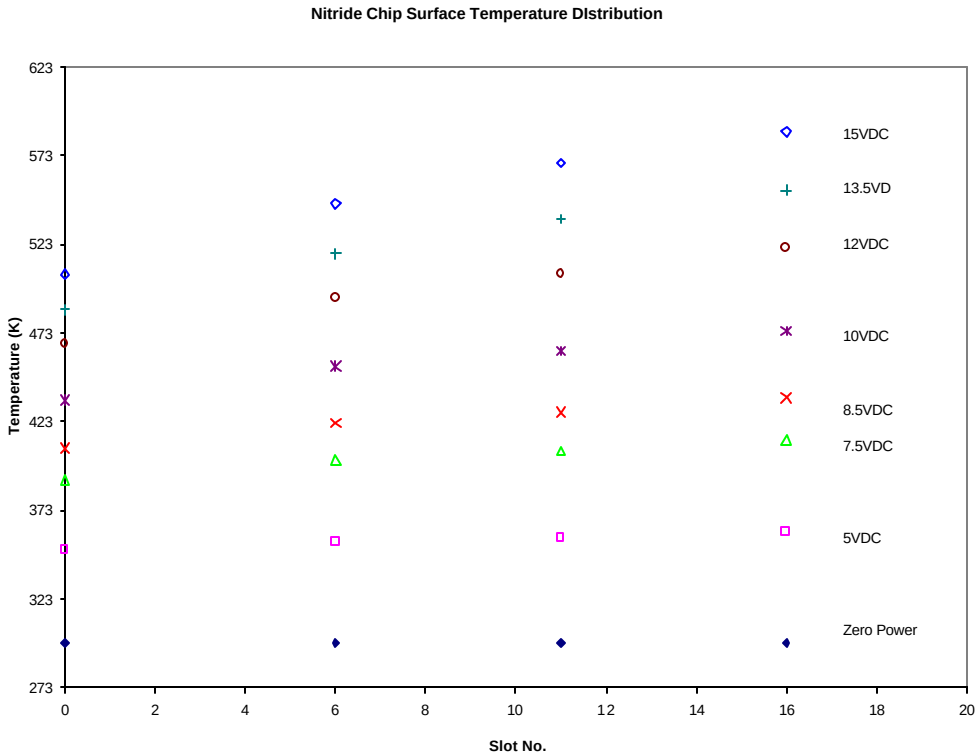

Figure 18 – Nitride heater chip surface temperature distribution based on slot location. Center of the chip lies between slot 18 and 19. The data points are drawn as large as the largest error (±2.6K) of the ensemble averages.

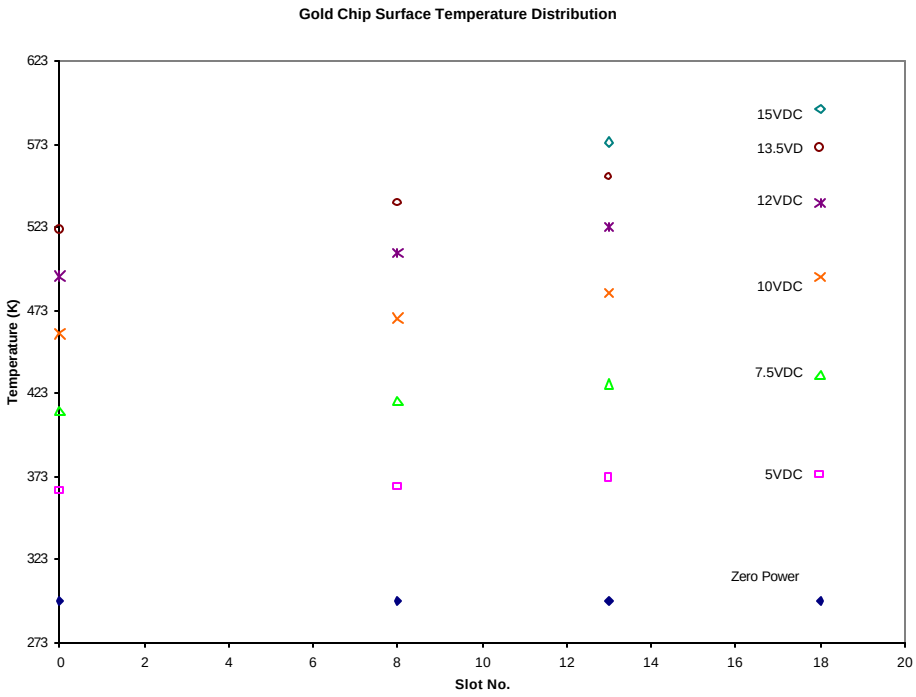

Figure 19 – Gold heater chip surface temperature distribution based on slot location. The data points are drawn as large as the largest error (±3.4K) of the ensemble averages.

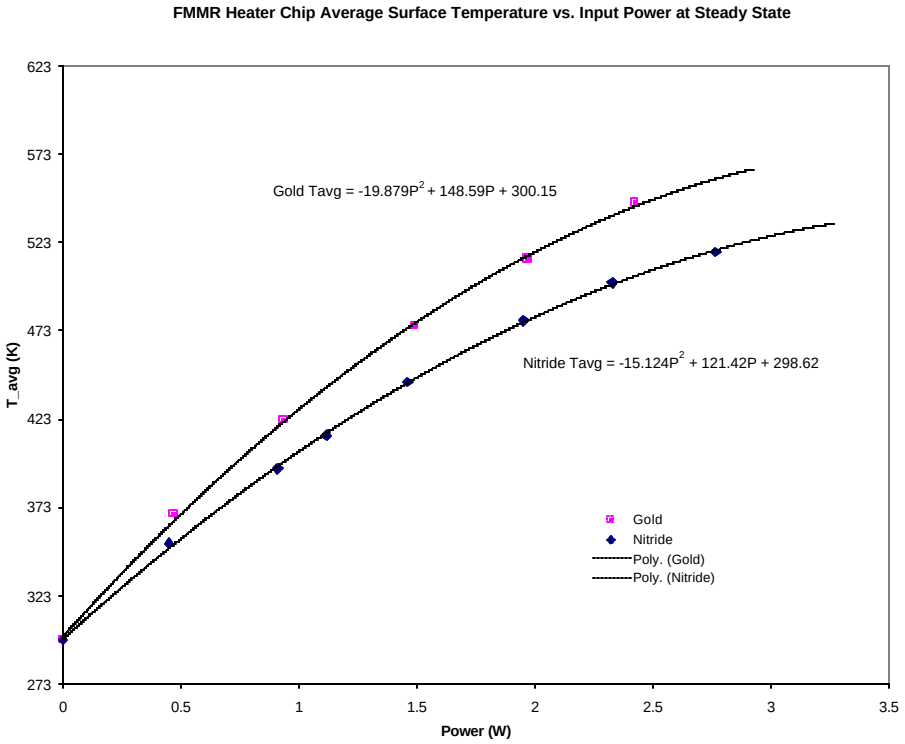

Figure 20 – Comparison of the average surface temperature of the gold and the nitride chip as a function of steady state input power.

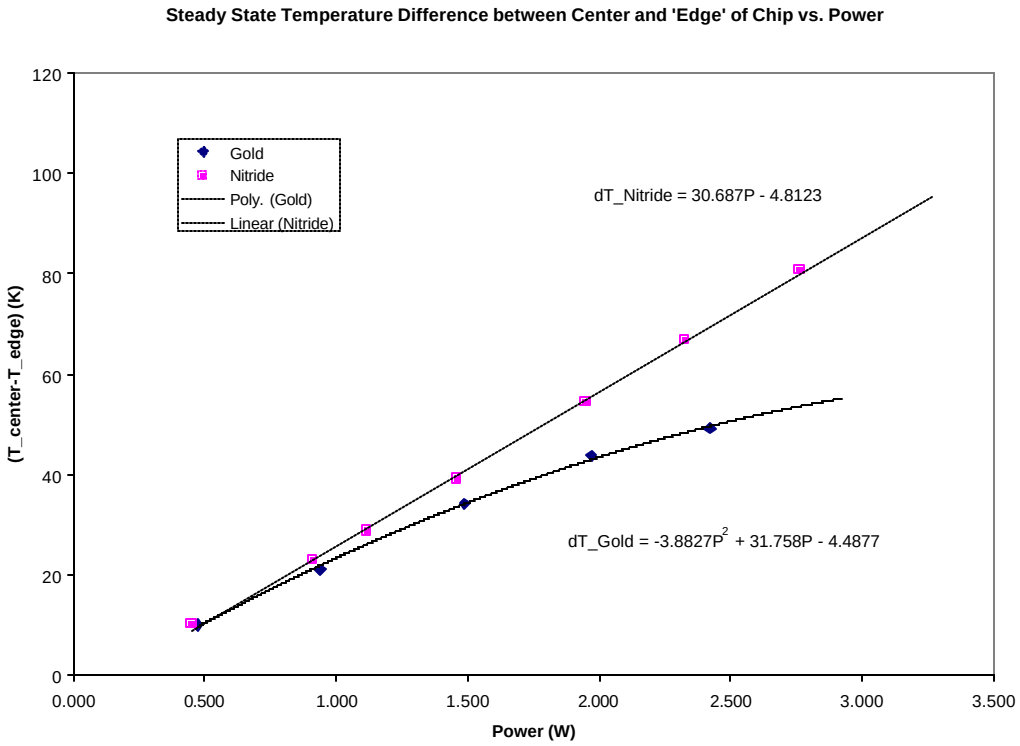

Figure 21 – Temperature difference between the center and the 'edge' of the nitride and the gold chip in high vacuum.

This result implies that the temperature gradient on the heater chip is different between the gold and the nitride chip. The conjecture can be verified by plotting the temperature difference between different thermocouples. Figure 21 shows the difference in temperature between the center and the edge (where contact with top Teflon housing begins) of the nitride and the gold chip.

The temperature difference in the nitride chip increases with input power in a linear fashion, while the trend in the gold chip is definitely nonlinear. Interestingly, the change also appears to decrease with respect to input power at high temperature for the gold chip. This could be contributed to the presence of the gold layer on the backside for several reasons. First, the gold layer could act as a thermal conduction blanket, which improves the temperature distribution of the chip. Second, the gold layer on the back is connected to the #0-80 electrical connection through the silver epoxy and the silicon wafer by nature of the manufacturing process, and thus, acts as a backside heater.

Although the ohmic resistance might be insignificant compared to the heating element in front, it still contributes to the overall heat transfer process of the chip. A comparison of the voltage drop across the two chips at the same power supply voltage setting would infer to the presence of a "different" heating element. Figure 22 is a plot showing the typical voltage across the gold and the nitride chip at 13.5VDC. Notice the nitride chip voltage decreases with time because the resistance of the heating element increases with temperature. The voltage of the gold chip, however, seems to oscillate gently with time and does not decrease with increasing temperature. The electrical connection between the heater, the silicon layer and the back coating was not intended in the design. It is interesting to observe its coupled effects with temperature in the experiment; however, efforts to enforce the electrical insulation between the different layers will be made in the design of the next generation FMMR heater chip.

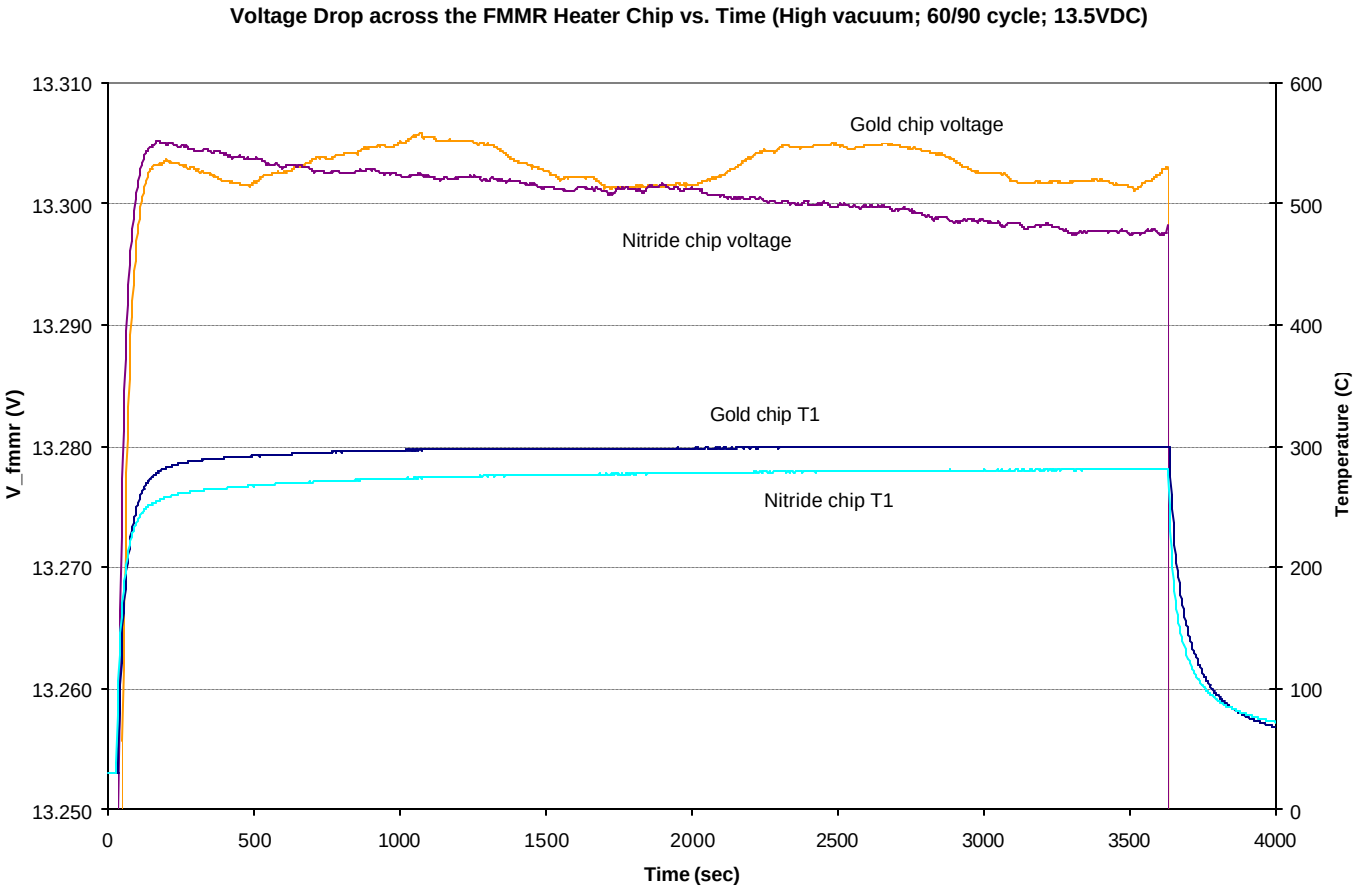

Figure 22 – Voltage drop across the gold and the nitride chip.

Set 3: High Vacuum, Cold Environment Power Variation

The result of the nitride chip operating at various voltages at low vacuum (2e-8Torr < background pressure < 5e-8Torr) inside the thermal shroud with liquid nitrogen cooling is summarized in Figure 23. The result of the gold chip is displayed in Figure 24.

Figure 25 compares the nitride chip average temperature radiating to a room temperature shroud and a LN2-cooled shroud. Figure 26 demonstrates the result for the gold chip. The average surface temperature of the gold chip varies linearly with input power, and the power lost to the environment is between 20 to 30%.

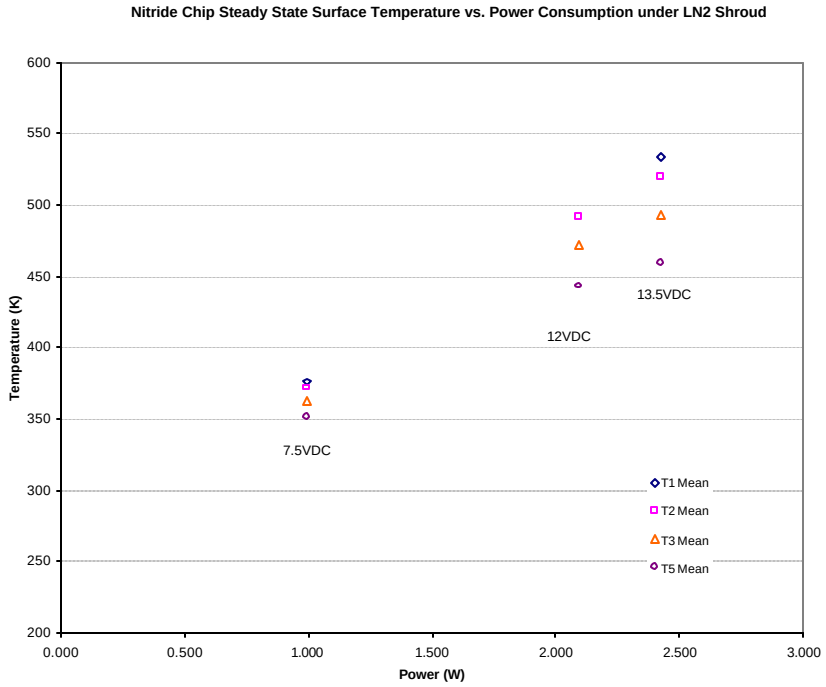

Figure 23 – Nitride chip surface temperature as a function of input power. The thermal shroud was maintained at 100K or lower. Thermocouple T4 was removed from the chip and mounted on the housing instead for this series of experiment. All T1 measurements of the 12VDC set had to be discarded due to a malfunction of the data acquisition system.

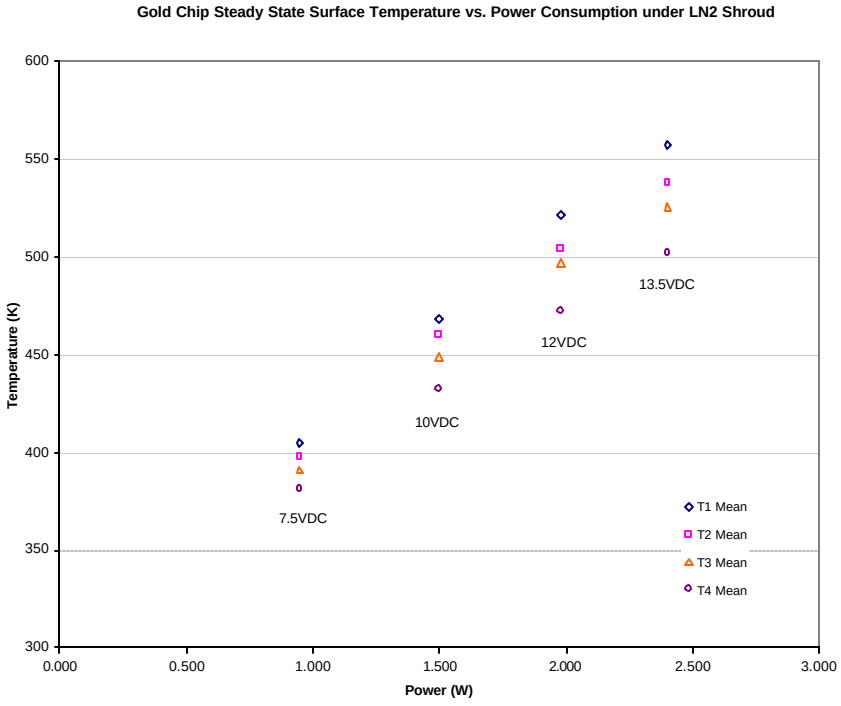

Figure 24 – Gold chip surface temperature as a function of input power. Thermal shroud surface temperature was maintained at 100K or lower.

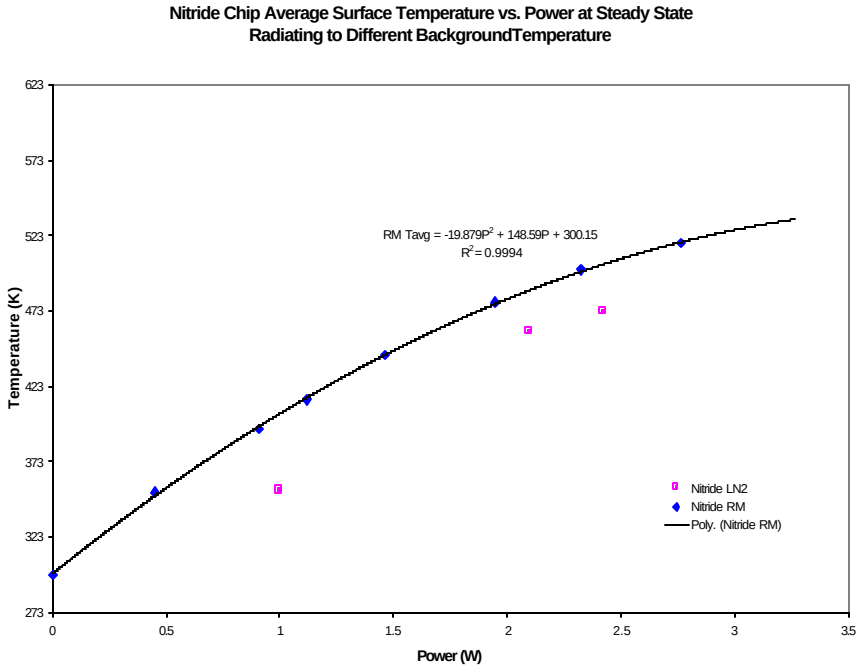

Figure 25 – Average surface temperature of the nitride chip radiating to room temperature and LN2-cooled thermal shroud.

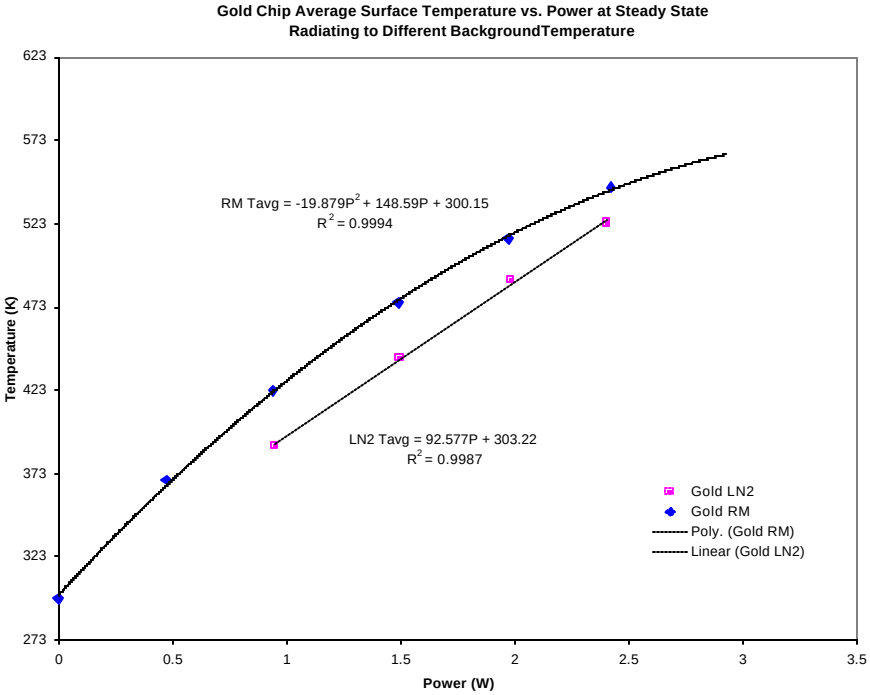

Figure 26 – Average surface temperature of the gold chip radiating to room temperature and LN2-cooled thermal shroud.

Preparing for Flight

Chip Characterization

The two flight units power consumption has been characterized prior to delivery. The characterization was carried out in high vacuum under the thermal shroud held at room temperature and with LN2 cooling. Voltage and current consumed during testing will be used to compare the flight data and to estimate the chip surface temperature.

Table 4 – Summary of the FMMR flight unit 1 chip characterization.

FLT1	Gold	Nitride
Room Temperature	2.420W	2.288W
LN2 Cooling	2.399W	2.316W

Table 5 – Summary of the FMMR flight unit 2 chip characterization.

FLT2	Gold	Nitride
Room Temperature	2.506W	2.387W
LN2 Cooling	2.464W	2.417W

Functional Testing

Two basic functional tests are to be carried out on the flight units before and after various environmental testing and spacecraft integration. The continuity test is simply to check the resistance of the chips to make sure that they are not broken and the electrical connection is intact. High vacuum functional testing is similar to chip characterization experiment, but the operation cycle may be different. The test units are also tested on the bench with the flight electrical and power subsystem and software prior to flight components integration. Once the flight integration is complete, FMMR functionality testing will become part of the spacecraft functionality test.

Environmental Testing

The engineering unit (EU) of the FMMR flight experiment has gone through random vibration testing. The test standard is taken out of the Space Shuttle HitchHiker's User's Guide. Visual inspection at 1, 10X and 25X and continuity test were carried out immediately before and after vibration testing. Functional testing at high vacuum was also carried out when the EU came back to the vacuum facility. No structural damage was discovered due to the vibration test.

For the flight units, they will be subjected to sine burst, random vibration and thermal vacuum with the flight spacecraft in the middle of October, 2001.

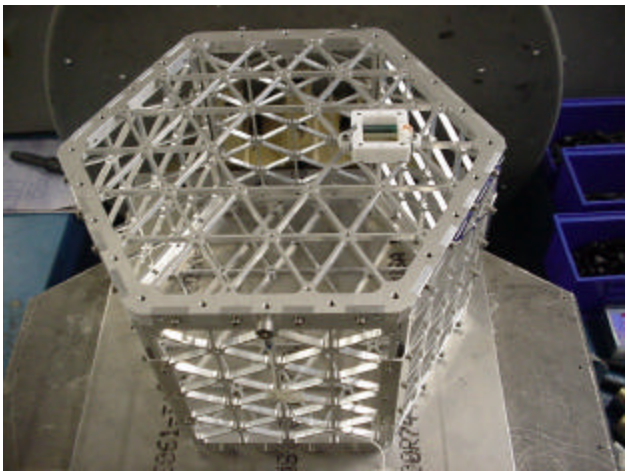

Figure 27 – FMMR EU mounted on the spacecraft development isogrid structure for x-y direction random vibration testing.

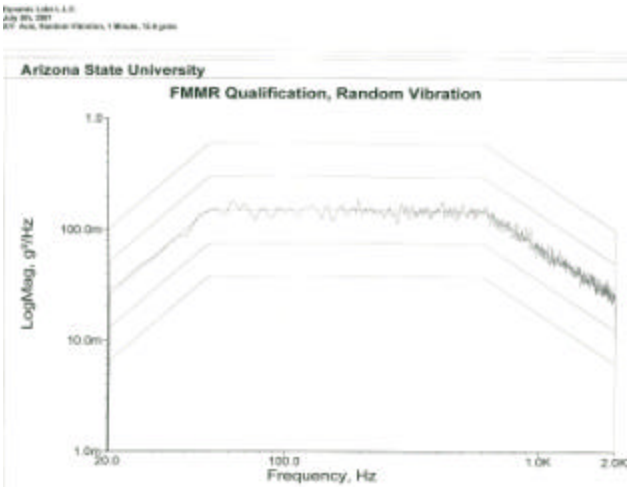

Figure 28 – Test profile recorded by the accelerometer on the isogrid structure for the x-y random vibration.

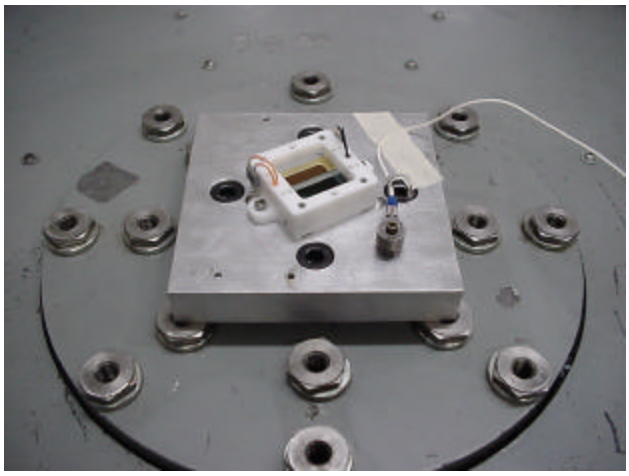

Figure 29 – FMMR EU mounted on the shake table with an aluminum fixture for z-axis random vibration testing.

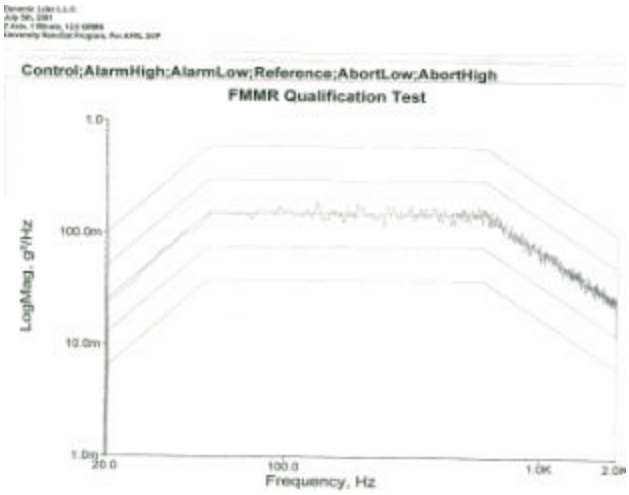

Figure 30 – Test profile recorded by the accelerometer on the test fixture for the z-axis random vibration.

Conclusions

Chip Characteristics

The gold and the nitride FMMR heater chips were tested in laboratory. Their surface temperature and power consumption were characterized in high vacuum at room temperature and under a LN2-cooled thermal shroud. The gold chip appears to be more power efficient compared to the nitride chip, even though extrapolation of experiment data projects that the power consumption for the chips to reach 600K is approximately 2.9W. The gold fares better not only because the surface temperature is higher than the nitride chip for a given power, the temperature gradient across the chip is also smaller. Hence, the overall surface temperature of the gold chip is higher than the nitride chip. This would certainly benefit the thrust produced by the gold FMMR heater chip.

Flight Preparation

The FMMR experiment engineering model has been through random vibration test to the standard identified in the Shuttle Hitchiker's User's Guide. No physical damage has been observed in the post-random vibe functional testing. The flight units will go through the same test on the flight spacecrafts as part of the flight qualification testing.

Acknowledgement

Hearty thanks to all my labmates at USC for their laughs and help, and especially to Bjorn Bjelde and Marc Young for helping me move all the LN2 bottles and lift the chamber lid, and the occasional insanity check and counseling thereof.

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